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INFORMS Seminar Series

Spatial Dirichlet Process Modeling based Statistical Control Scheme and its Application for Geometric Quality Assurance with Wafer Thickness Profiles

SEMINAR SESSION INFORMATION

DATE: Wednesday, March 29

TIME: 12:15pm

LOCATION: Durham 260

PROVIDED: Pizza and Soda

SPEAKER INFORMATION

Jia (Peter) Liu
PhD Candidate

Grado Department of Industrial & Systems Engineering

MEMBERSHIP INFORMATION

Fees are as follows and include all weekly seminars (12+) & workshops.

FIRST MEETING: FREE

MEETING: $5

SEMESTER: $25

As raw materials for manufacturing integrated circuits, high-quality semiconductor wafer products are the prerequisite for the advancement of electronic products and Internet-based technologies. The current industrial practice uses the summary quality features for quantifying wafer thickness, such as total thickness variation, bow, and warp, which, however, underuse the abundant profile measurements and may lead to inconsistent product quality assurance. The existing spatial modeling and statistical quality control schemes for wafer thickness profiles do not take into account the clustering phenomenon among the wafers, therefore are insensitive to out-of-control wafers.

By marrying spatial statistics and Dirichlet process, we proposed spatial Dirichlet process (SDP) modeling which utilizes the spatial clustering phenomenon existing in wafer thickness profile data. A key advantage of the proposed SDP modeling stems from its adaptive means in determining the clusters in the spatial data by using Dirichlet process modeling with a nonparametric and data-driven nature. Consequently the developed SDP-based statistical control scheme can detect the aberrant spatial data with higher power of test than the state of the art benchmark method.

Questions? Comments? Send an e-mail to shafae1@vt.edu

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